REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-2 and 4-17 are presently active in this case, Claims 12, 16 and 17 are amended by way of the present amendment.

In the outstanding Office Action, Claims 16 and 17 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite; Claims 1, 2, 4, 5, 6 and 11-13 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. 6,333,857 to Kanbe et al.; and Claims 8, 9 and 14-17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kanbe et al. in view of U.S. 6,323,435 to Strandberg.

With regard to the rejection under 35 U.S.C. § 112, second paragraph, Applicants have amended the claims to correct informalities noted in the outstanding Office Action. Therefore, the rejection under 35 U.S.C. § 112, second paragraph, is believed to be overcome.

As discussed in the response filed November 13, 2008, Claim 1 recites that a distance between the ground through hole and the power through hole is in a range of 60 to 550 μm. The Office Action admits that Kanbe et al. does not disclose this feature, but states

> . . . the distance will be decided based on the space available in the board to avoid shorting of the adjacent pad on via during operation as well as better routing of the traces.[1]

Further, the Office Action states that

> [T]here are various criteria for maintaining distance between the via holes. One of the criteria is to keep a distance to avoid shorting of the adjacent pad on via during operation or during solder connection or to help better routing of the traces. Use of laminated capacitor does not exclude other criteria to be met.[2]

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[1] Office Action at paragraph linking pages 3-4.
[2] Office Action at Response to Arguments portion, page 8.

Applicants traverse this assertion.

As discussed in Applicants' specification, an IC chip utilizing high switching frequency (for example 5GHz) is prone to switching errors. However, when loop inductance of the printed circuit board for mounting the IC chip is lower than 60pH, IC chip errors can be reduced. Based on this fact, the present inventor conducted studies and experiments to determine a relationship between loop inductance and distance between the ground through hole and power through hole. Based on such research, the inventor discovered that a distance between ground and power through holes of 60 to 550 μm can provide desired loop inductance and therefore reduce switching errors, even at high switching speeds of 3Ghz or more. This is discussed throughout Applicants' specification, and data relating to these experiments is shown in Fig. 16.[3]

As discussed in the November 8th response, Kanbe et al. utilizes the laminated capacitor in the core substrate to solve the problem of noise or delay of power supply to the IC chip which causes switch errors. Therefore, there is no need in Kanbe et al. to provide a particular distance requirement between the power and ground through holes. Thus, Kanbe et al. clearly does not show or suggest any particular distance range between the power and ground through holes. Indeed, since Kanbe et al. forms a laminated capacitor in the core substrate, if the distance between the through-holes is reduced, an effective area of the capacitor electrode (area of the metal layer between adjoin through-hole) is reduced. This would create a problem of reduced capacitance in Kanbe et al.

Further, in Kanbe et al., by checking the character and short-circuit of the laminated capacitor in the core substrate, it is possible to use only the checked core substrate so that a yield rate can be improved. That is, in Kanbe et al, the laminated capacitor in the core substrate becomes an indispensably necessary condition in order to improve the yield rate.

[3] Applicant's specification at pages 3, lines 16-19 and page 6, lines 5-10.

Applicants submit that one of ordinary skill in the art would never imagine from this reference the idea that narrowing the pitch of the through holes can obtain the effect of cancellation of the induced electromotive force occurring in the ground through holes and the power through holes. Further, as noted above, since Kanbe et al. forms the laminated capacitor in core substrate, if the distance between the through hole is narrower, the effective area of electrode (area of the metal layer between adjoin through hole) of the capacitor is reduced and capacitance of capacitor is reduced. Kanbe would have a problem of reducing the capacitance of the capacitor, if the distance of through hole in Kanbe et al. is made narrower as in the present invention.

Stadberg does not show the distance between the through hole, and the placement of the glad through hole and the power through hole. Therefore, Stadberg cannot find the optimum value of distance of through holes.

Thus, even if Kanbe and Stadberg can be combined, the present invention cannot be constructed.

Consequently, in view of the present amendment, no further issues are believed to be outstanding in the present application and the present application is believed to be in condition for formal allowance. An early and favorable action is therefore respectfully requested.

Respectfully submitted,

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